Please add the following new claims:

30. **(New)** a non-volatile memory array, comprising:

a plurality of memory cells arranged in at least a first row of memory cells and a second row of memory cells adjacent to the first row, each of the memory cells along a portion of the first row sharing a common source with at least one memory cell of the second row; and

a conductive member being disposed along at least a portion of the first and second rows, said conductive member being associated with the first and second rows and making contact with the common sources of the memory cells in said portion of the rows, the contact of said conductive member being self-aligned with the memory cells of said portion of the rows,

wherein said conductive member enables the selection of one of the first or second rows during an erase operation.

31. **(New)** The non-volatile memory array of claim **30**, wherein each of said memory cells including a drain region, a source region, a channel region disposed between the drain region and the source region, a floating gate disposed over at least the channel region, and a control gate disposed over the floating gates, the control gates of the memory cell in each row being commonly coupled to a word line extending generally parallel to the row; and the conductive member being disposed generally parallel to the word line along at least portion of its respective row.

32. **(New)** The non-volatile memory array of claim **30**, wherein said conductive member includes polysilicon.

33. **(New)** The non-volatile memory array of claim **32**, wherein said conductive member includes a metal silicide.

34. **(New)** The non-volatile memory array of claim **32**, wherein said conductive member includes a metal.

REMARKS

Claims 1-29 remain in this application for further consideration by the Examiner. In the above-identified Office Action, the Examiner rejected claims 1-6, 10-14, 17-18, 20-22, and 24-29 under 35 U.S.C. §103(a) as being unpatentable over Sung et al. "Sung" and rejected claims 7-9, 15-16, 19, and 23 under 35 U.S.C. §103(a) over Sung, in view of Shrivastava and Juengling.

In the following paragraphs, Applicants will address the objection to the specification and the rejection of the claims separately.

AMENDMENT TO THE SPECIFICATION

The specification has been amended to rectify a typographical error. Applicant submits that no new mater has been introduced in the present Application by this amendment.

AMENDMENT TO THE CLAIMS

Claims 1, 2, 13, 17, 20-24, and 25-29 have been amended to more clearly claim what the Applicants regard as their invention.

Claim 1 has been amended to rectify a typographical error. It has further amended to more clearly claim that the conductive member is associated with the row. Applicants submit that no new matter has been introduced by this amendment.

Claim 2 has been amended to more clearly claim that the conductive member is associated with the adjacent row pair. Applicants submit that no new matter has been introduced by this amendment.

Claim 13 has been amended to incorporate the limitations of the originally filed claim 19. It has further been amended to claim that the conductive member is associated with a first row of memory cells to which the first flash EPROM cell belongs. In addition, the conductive member enables the selective erasing of the memory cells of the first row. The support for this amendment is provided in the specification, specifically Figs. 2a-2c and the related descriptions. Applicants submit that no new matter has been introduced by this amendment.

Claim 17 has been amended to incorporate the limitation of the originally filed claim 18. It has further been amended to claim that the conductive member is associated with a second row of memory cells that is adjacent to the first row and to which the second flash EPROM cell belongs. In addition, the conductive member enables the selective erasing of the memory cells of the first row, the second row, or both rows during an erase operation. The support for this amendment is provided in the specification, specifically Figs. 2a-2c and the related description. Applicants submit that no new matter has been introduced by this amendment.

Claim 20 has been amended to more clearly claim the present invention and to incorporate the limitation of claim 25. The support for this amendment is provided in the specification and accompanying drawings. Applicants submit that no new matter has been introduced by this amendment.

Claim 21 has been amended to more clearly claim the programmability of the memory of the present invention. The support for this amendment is provided in the specification, specifically on pages 4 and 13-16 and the accompanying drawings. Applicants submit that t no new matter has been introduced by this amendment.

Claims 22-29 have been amended to use a more consistent claim language in view of the amendment to claim 20. Applicants submit that t no new matter has been introduced by this amendment.

In view of the above, Applicants submit that no new matter has been introduced by the amendments to the claims.

NEW CLAIMS

New claims 30-34 have been added in this application. Applicants submit that no new matter has been introduced by the addition of the new claims 30-34.

The new independent claim 30 claims a non-volatile memory array that includes a plurality of memory cells arranged in at least two adjacent rows. Each memory cell in the first row shares its source with one memory cell of the second row. The array further includes a conductive member that makes contact with the common sources and is self aligned with the memory cells of the rows. The conductive member enables the selection of either of the two rows during an erase operation. The support for this claim has been provided in the specification and the accompanying drawings. Applicants submit that t no new matter has been introduced by this amendment.

The new dependent claim 31 depends on claim 30 and further defines the elements of the array of claim 30. The support for this claim has been provided in the specification and the accompanying drawings. Applicants submit that t no new matter has been introduced by this amendment.

The new dependent claims 32-34 directly or indirectly depend on claim 30. Each of the new claims further defines the conductive member of claim 30. The support for this claim has been provided in the specification and the accompanying drawings. Applicants submit that t no new matter has been introduced by this amendment.

In view of the above, Applicants submit that no new matter has been introduced by the new claims.

REJECTION UNDER 35 USC §103(a)

On page 2 of the above-identified Office Action, the Examiner rejected claims 1-6, 10-14, 17-18, 20-22, and 24-29 under 35 USC §103(a) as being unpatentable over Sung et al. ("Sung"). Applicant respectfully traverses the Examiner's position for the following reasons. However, before presenting the arguments, Applicants believe that a brief description of the present invention would be beneficial.

The present invention relates to non-volatile memories, specially to flash EPROMs. A memory array according to the present invention includes memory cells that are arranged in rows and columns. The memory cells in each adjacent row pairs have common sources. A source conductor member is provided for each row pairs. Each source conductor member makes contact with each common source of the respective row pairs. Each source conductor is self-aligned with the edges of the bit lines of the adjacent memory cells. Referring to Fig. 2c of the present application, it is clearly shown that the source conductor 120a is self-aligned to the sidewall spacers 144 of the two memory cells shown in this figure.

Referring to Figs. 2a and 2c, the source conductor 120a is shown to be a single conductive layer that makes contact with the common sources of the memory cells of the adjacent row pairs on the top section of Fig. 2a. However, it is also shown in Fig. 2a that each source conductive member is isolated from the adjacent source conductive member. Each conductive member extends in the same direction as the rows.

The architecture of the present invention has several advantages over the prior art architectures. Unlike prior art flash EPROM architectures, the architecture of the present invention provides an EPROM array having very low resistance source lines running in the row direction. For example, the sheet resistance of the source interconnect can be reduced from about 80Ω/ to 8Ω/ using the present invention. As a result the number of metal "straps" required to provide a reference voltage to the source lines can be eliminated or reduced, freeing up area in the array. (See page 13, lines 27-32, of the specification)

In addition, the architecture of the present invention allows the array to be broken into customizable groups of one or more rows by source decoding. In this manner, a user may selectively erase various sectors of arbitrary sizes (i.e., programmable erase granularity). For example, in prior art approaches, to erase selected rows in a given common source region (or "sector") the entire common source region (i.e., all the sources in the sector) would be driven to a source erase voltage (a positive voltage, for example) while selected word lines (those rows that are to be erased) were driven to a word line erase voltage (a relatively large negative voltage, for

example). Those rows within the sector that were not to be erased would have word lines driven to word line de-select voltage, but would still have their sources driven to the source erase voltage. In contrast, by using decoded sources, the present architecture allows the word lines and sources of only those rows that are to be erased, to be driven to the word line erase voltage and source erase voltage, respectively. The number of rows that may be erased in this manner is not limited to a certain minimum number due to a common source diffusion, but can be determined by a user of the flash EPROM device. Such architecture provides the selectable erase advantages over the conventional EEPROMs, while providing the rapid erase advantages of conventional flash EPROMs. Providing this new flexibility can also improve reliability by better control of erase, and erase convergence techniques. (See pages 13, line 33 through page 14, line 15,of the specification)

As it is understood by the Applicants, the invention in the Sung relates to "electrical connections to bit lines in memory devices." (Column 1, lines 13-14) It does not discuss or teach an architecture that focuses on the source connections. Sung provides a memory architecture in which tungsten plugs 40 and 40'are used to provide access to the drain region 26 and source region 27, respectively. (See Fig. 2I). Thereafter, a layer of intermetal dielectric 42 is formed on the device as shown Fig. 2I. Openings to the drain plugs 40 are then created. Thereafter, the metal bit line material 44 is deposited as a blanket layer over the layer 42. It is then etched to provide the metal bit line 42. The bit lines 44 does not contact the source plugs 40' since the dielectric regions 42 separate the bit lines 44 from the source lines 40'. (See column 3, lines 37-46)

As mentioned above, the present invention focuses on the self-aligned source connections. Each source connection is associated with a pair of adjacent rows and are isolated from the other source connections. Thus, the architecture of the present invention is patently different from that of Sung. Typically, the bit lines are used to program and the source lines are used to erase the memory cells, the architectures focusing on the bit lines are different from those focusing on the source connections. Namely, the bit line connections would require a larger space than the source line connections.

On page 2 of the above-identified Office Action, the Examiner has rejected claims 1-6, 10-14, 17-18, 20-22, and 24-29 under 35 U.S.C. §103(a) as being unpatentable over Sung. The Examiner stated that "...Figure IA shows a plurality of memory cells having regions as claimed, with insulating sidewalls 29', and with conductive member 40' making contact with the sources of the memory cells. Each source is shared by two adjacent transistors, and thus each source

would be common to cells in two adjacent rows. Each device structure as claimed appears in the Sung figures."

Applicants respectfully disagree with the Examiner. The device of Sung does not show a source connection that is connected to the sources of the memory cells of two adjacent rows and is isolated from the other source connections. In fact since the Sung reference focuses on the bit liner connections, refer to the above, it does not teach any specific details of the source lines. Typically, the sources in the prior art devices are all commonly connected. Since, the reference fails to provide any details about the source connections, Applicants believe that the sources of its device are all commonly connected. This is not true with the present invention.

The device of the claims 1-12 all include a conductor member that is connected to sources of one or a pair of rows and are associated with the one row pairs. This architecture provides the capability of selectively erasing one or a number of rows in the array of the present invention while not affecting the memory cells in the non-selected rows.

The architecture of Sung does not provide the capability of selectively erasing one or more rows of memory cells since it does not teach the source conductive members that connect to the sources of memory cells of adjacent row pair and are independent from each other.

In view of the above, Applicants submit that the Sung reference does not reach or render the present invention obvious.

The amended claim 13 claims a flash EPROM device, the source of which is connected to a conductive member. The conductive member is associated with a first row of memory cells to which the first flash EPROM cell belongs. In addition, the conductive member enables the selective erasing of the memory cells of the first row. As argued above, this is not shown or taught by the Sung reference. Thus, the amended claim 13 is not anticipated nor is it rendered obvious by the Sung reference.

Claims 14-16, the amended claim 17, and claims 18-9 depend on the amended claim 13 and include the limitation of the independent claim 13. Thus, the above arguments equally apply to these claims. Accordingly, claims 14-16, the amended claim 17, and claims 18-9 are not anticipated nor are they rendered obvious by the Sung reference.

The amended claim 20 claims a flash EPROM memory device that includes,

> "... a plurality of source connecting members extending in the row direction, each of said source connecting members disposed over, and making contact with, sources of memory cells of each adjacent pair of rows,
> wherein each of said source connecting members enabling the selective erasing of the memory cells of one or both of the corresponding rows during an erase operation."

This limitation is similar to those of the independent claims 1 and 13. Thus, the arguments provided for those claims equally apply here. Accordingly, the amended claim 20 is not anticipated nor is it rendered obvious by the Sung reference.

The amended claims 21-24 and 26-29 depend on the amended independent claim 20 and include the limitations of this claim. Thus, the arguments regarding claim 20 equally apply to these dependent claims. Accordingly, the amended claims 21-24 and 26-29 are not anticipated nor are they rendered obvious by the Sung reference

Claim 25 has been canceled in this response. Therefore, its rejection under section 103(a) will not be addressed here.

Regarding the dependent claims 25-29, the Examiner stated,

> "[c]ircuits performing functions as recited in claims 25-29 would have been obvious because the Sung device is intended to be used as a flash memory and the circuit functions recited would be needed to operate a flash memory." (Bottom of the page 2 and top of page 3 of the Office action)

Applicants respectfully disagree with the Examiner for the following reasons. First, as mentioned above, claims 26-29 are dependent on the amended independent claim 20 and, thus, include all the limitations of claim 20. The above arguments clearly show that Sung does not render these claims obvious. Second, since Sung does not teach a programmable architecture as the present invention does, it would not need the element that are claimed in the dependent claims 26-29. Thus, it would not have been obvious to incorporate such elements in a memory architecture in view of the teachings of Sung.

For the above stated reasons, Applicants submit that claims 26-29 are not rendered obvious by the Sung reference.

Since claim 25 has been cancelled in this Amendment, its rejection will not be addressed.

On page 3 of the above-mentioned Office Action, the Examiner rejected claims 7-9, 15-16, 19, and 23 under 35 U.S.C. §103(a) as being unpatentable over Sung in view of Shrivastava and Juengling. Applicants respectfully traverse the Examiner's position for the following reasons.

Claims 7-9 depend on the amended independent claim 1, and, thus, include all the limitation of this claim. Accordingly, the arguments presented with respect to claim 1 against the Sung reference equally apply to the dependent claims 7-9. Since the base reference Sung does not anticipate or render obvious claims 7-9, its combination with the Shrivastava and Juengling also will not render them obvious. Specially, in view of the fact that the Examiner is

relying on Shrivastava and Juengling for their alleged teachings of the use of polysilicon and double diffused layers.

Claims 15-16 and 19 depend on the amended independent claim 13. Accordingly, the arguments presented with respect to claim 13 against the Sung reference equally apply to the dependent claims 15-16 and 19. Since the base reference Sung does not anticipate or render obvious claims 15-16 and 19, its combination with the Shrivastava and Juengling also will not render them obvious. Specially, in view of the fact that the Examiner is relying on Shrivastava and Juengling for their alleged teachings of the use of polysilicon and double diffused layers.

Claim 123 depends on the amended independent claim 20. Accordingly, the arguments presented with respect to claim 20 against the Sung reference equally apply to the dependent claim 20. Since the base reference, Sung does not anticipate or render obvious claim 20, its combination with the Shrivastava and Juengling also will not render claim 20 obvious. Specially, in view of the fact that the Examiner is relying on Shrivastava and Juengling for their alleged teachings of the use of polysilicon and double diffused layers.

In view of the above, Applicants submit that claims 7-9, 15-16, 19 and 23 are not rendered obvious by the Sung reference in view of Shrivastava and Juengling.

NEW CLAIMS 30-34

The new claim 30 also includes,

> "... a conductive member being disposed along at least a portion of the first and second rows, said conductive member being associated with the first and second rows and making contact with the common sources of the memory cells in said portion of the rows, the contact of said conductive member being self-aligned with the memory cells of said portion of the rows, wherein said conductive member enables the selection of one of the first or second rows during an erase operation."

Again, this limitation is not taught by the Sung reference itself, or in combination with Shrivastava and Juengling. The above arguments equally apply to the new claim 30. Accordingly, claim 30 is not rendered obvious by the Sung reference along, or in combination with Shrivastava and Juengling.

The new claims 31-34 are dependent on the new claims 30 and, thus, include the limitations of the new claim 30. The above arguments equally apply to these claims. Accordingly, claims 31-34 are not rendered obvious by the Sung reference along, or in combination with Shrivastava and Juengling.

CONCLUSION

The claims 1-24, 26-34 remain in this application for reconsideration. For all the reasons set forth above, Applicants submit that all the remaining claims are now in condition for allowance. Thus, their speedy allowance is respectfully requested.

If the Examiner believes that a telephone conversation with the undersigned attorney of record would expedite the allowance of the remaining claims in this application, the Examiner is invited to contact the undersigned at the number listed below.

Respectfully Submitted,

A. Raissinia

Abdy Raissinia, Reg. No. 38,686

4/6/99

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